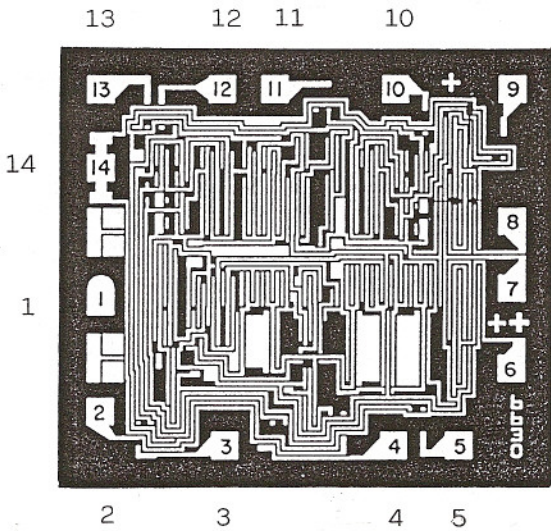




Sierra Components, Inc.

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Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.



<u>PAD NO</u>	<u>FUNCTIONS</u>
1	NC
2	RESET
3	J1
4	J2
5	J3
6	Q
7	VSS
8	Q
9	K3
10	K2
11	K1
12	CLOCK
13	SET
14	VDD

Top Material:
Backside Material:
Bond Pad Size:
Backside Potential:
Mask Ref:

APPROVED BY: MG

DIE SIZE : 75 x 66

DATE: 10/23/08

MFG: R.C.A.

THICKNESS:

P/N: CD4095BH